

PRIOR ART

FIG. 1

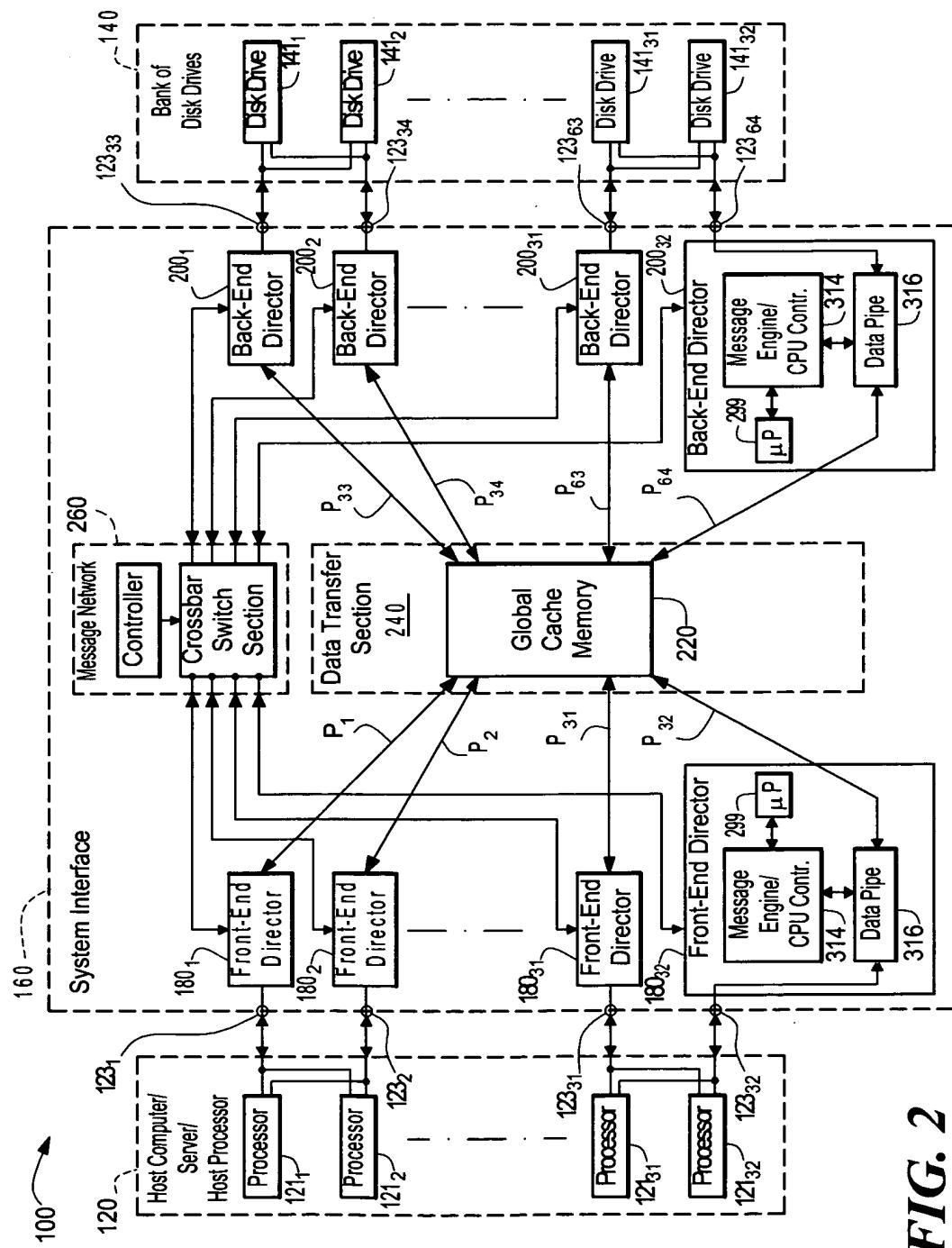
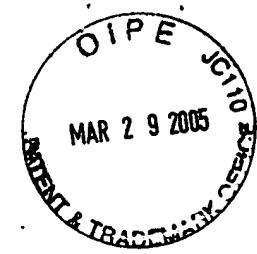


FIG. 2



3/30

FIG. 3

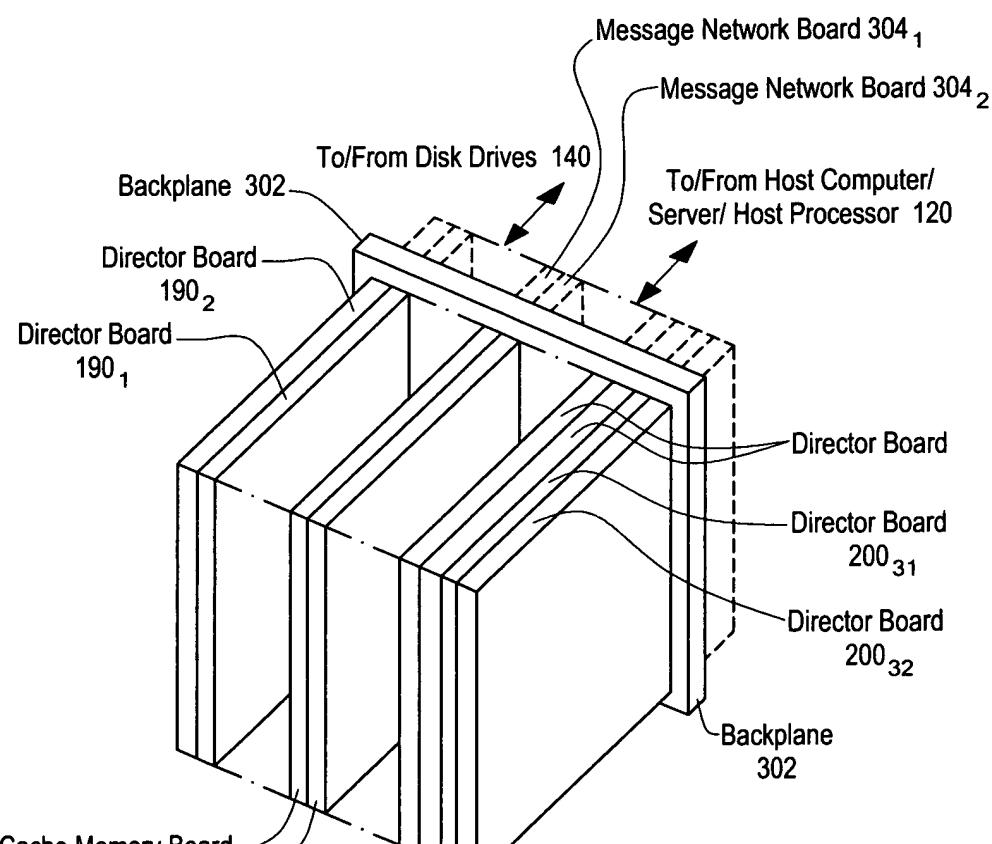
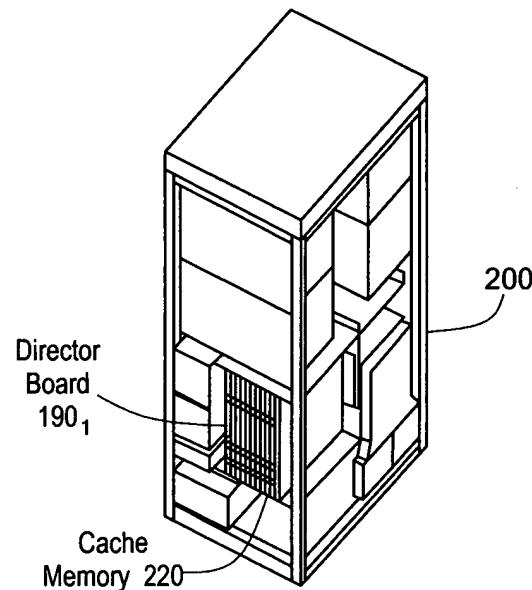
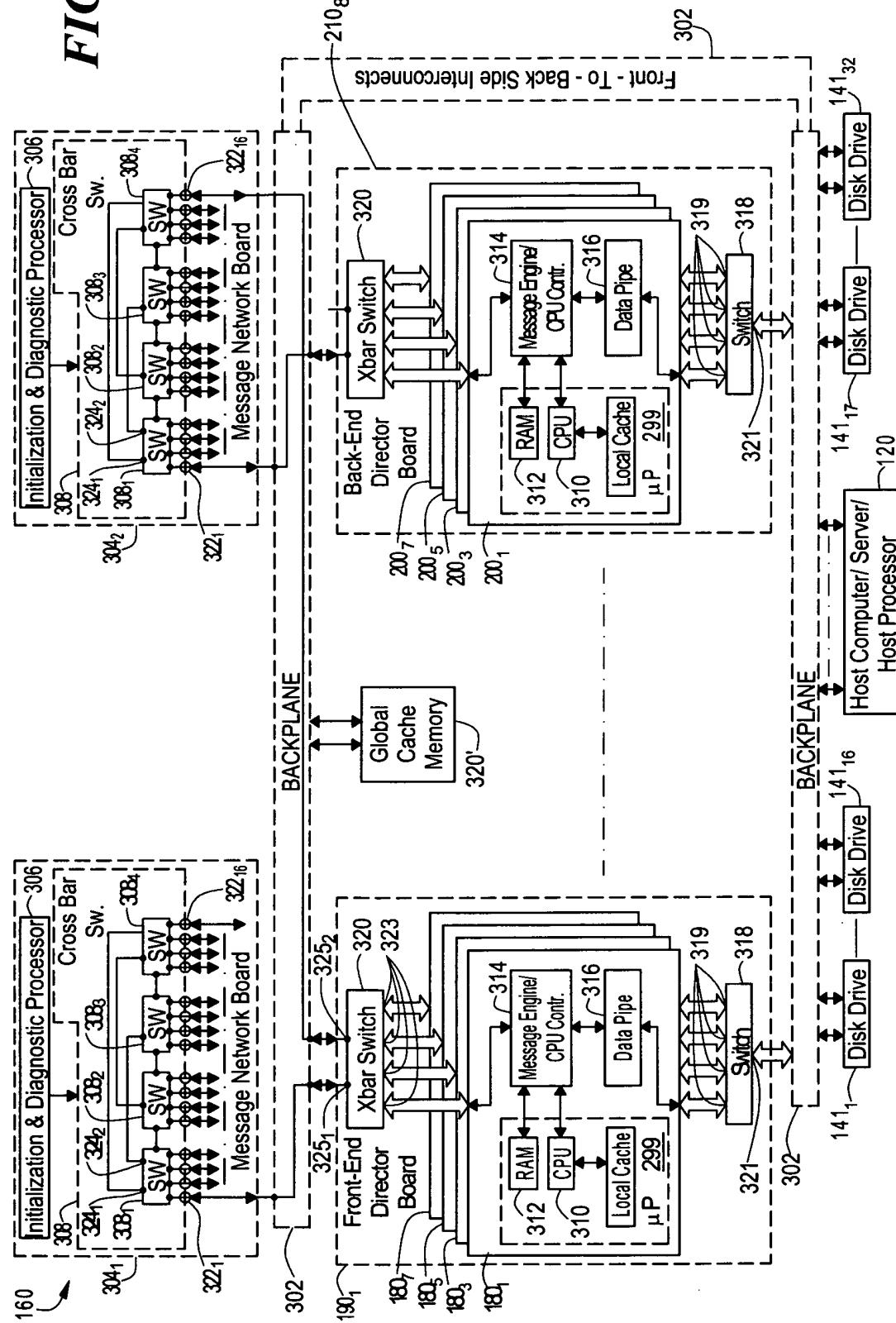


FIG. 4



FIG. 5



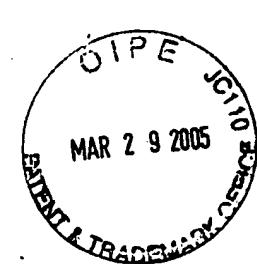


FIG. 6

FIG. 6A
FIG. 6B

5/30

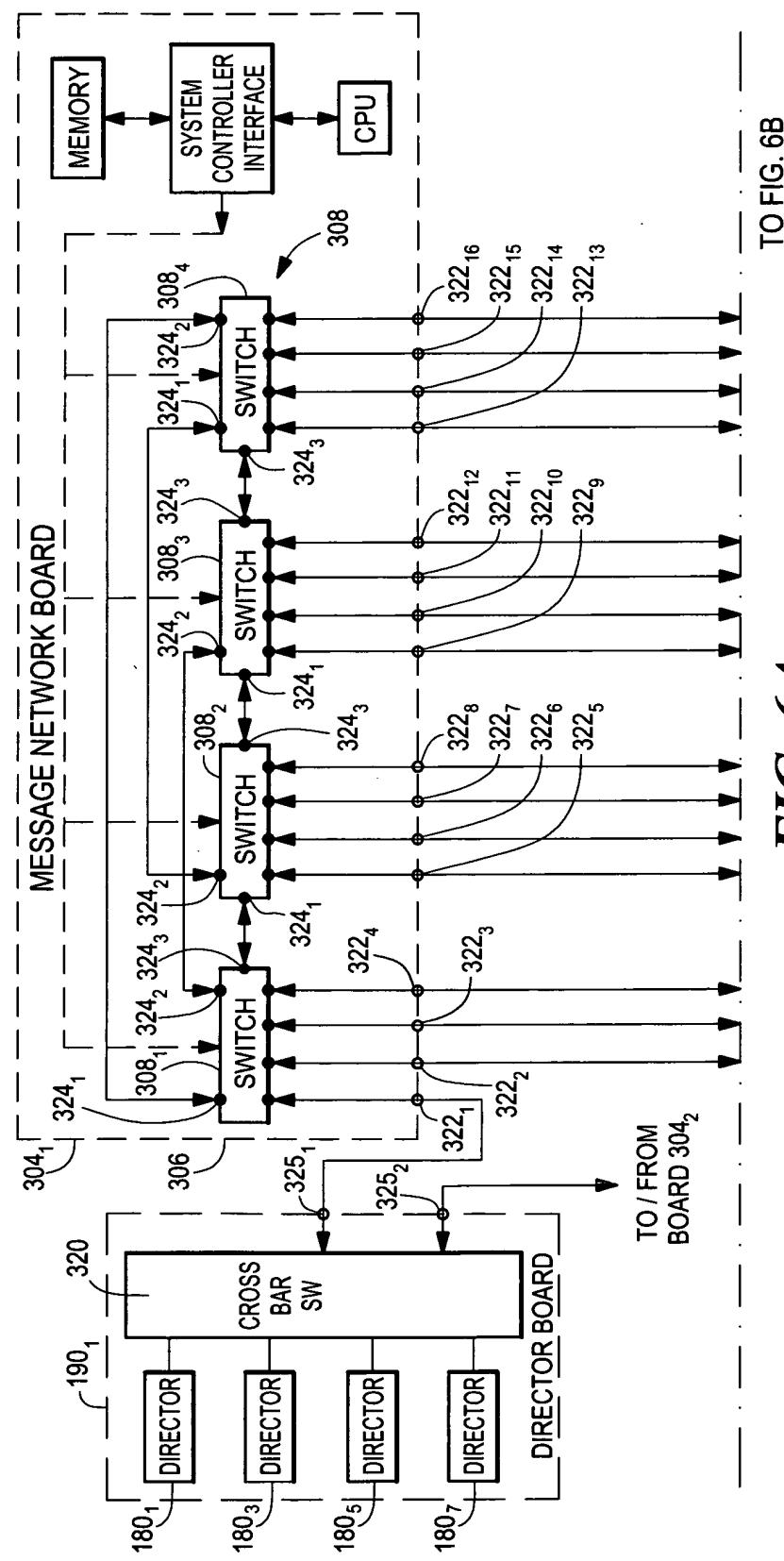


FIG. 6A

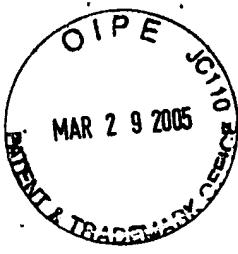
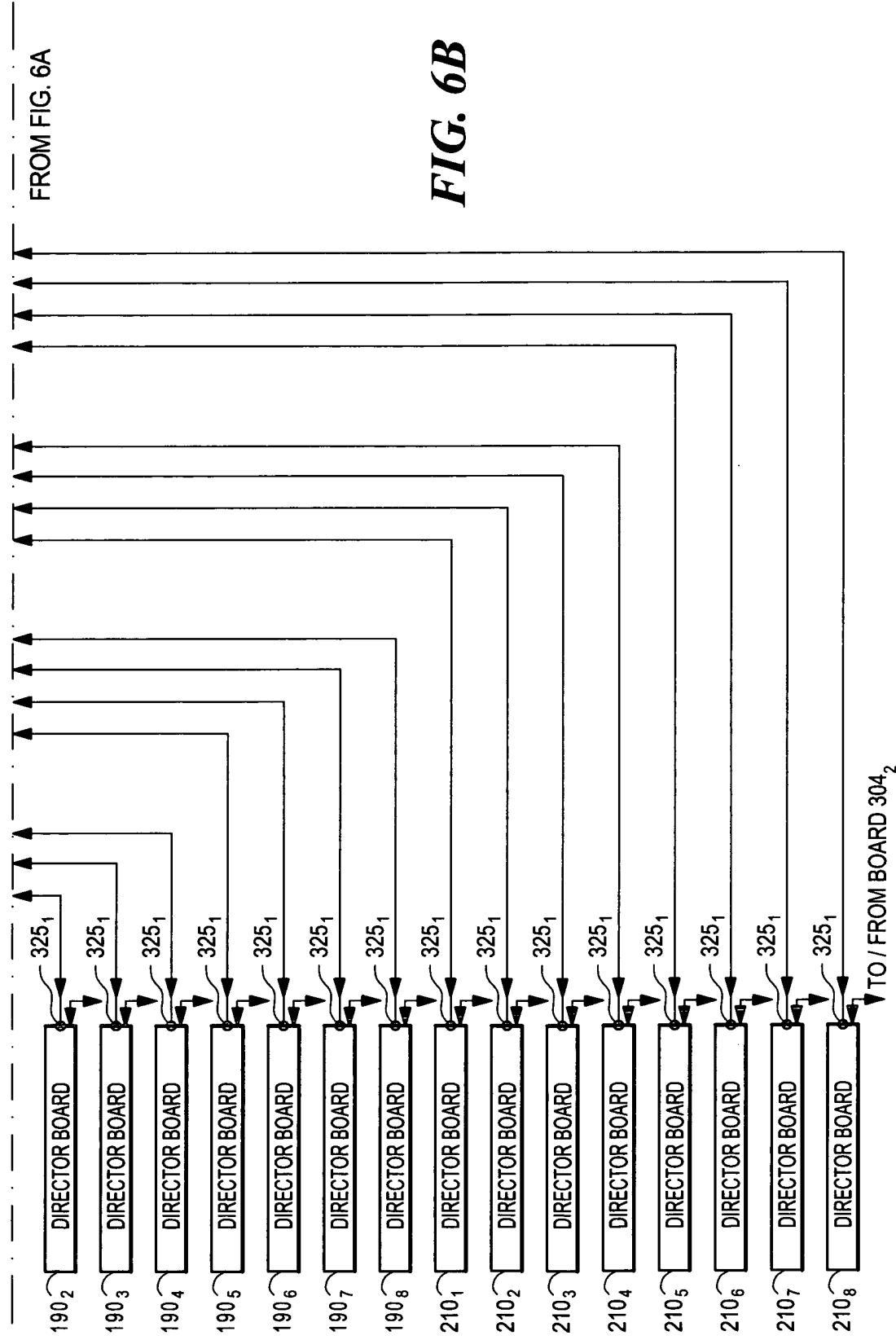


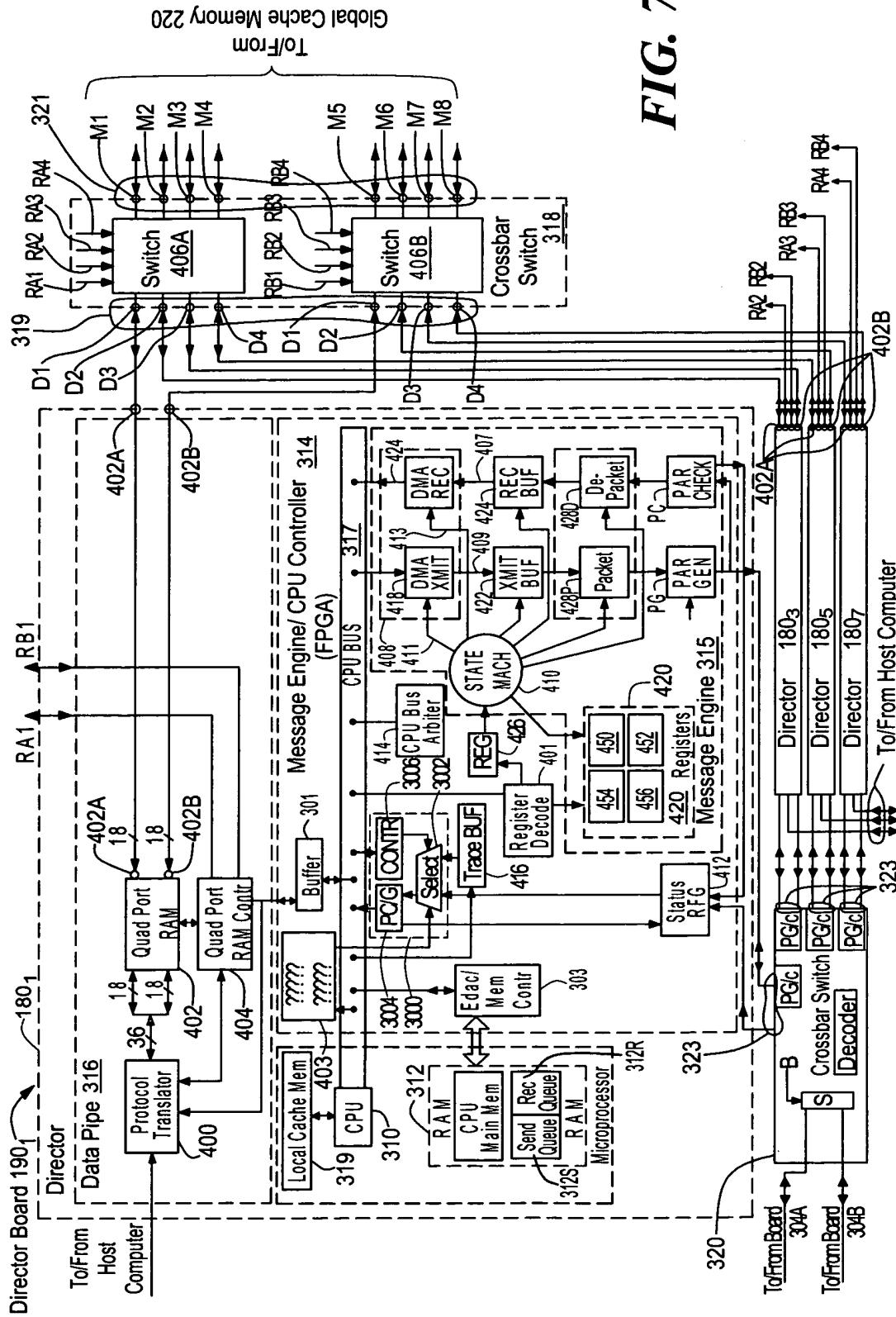
FIG. 6B





7/30

FIG. 7



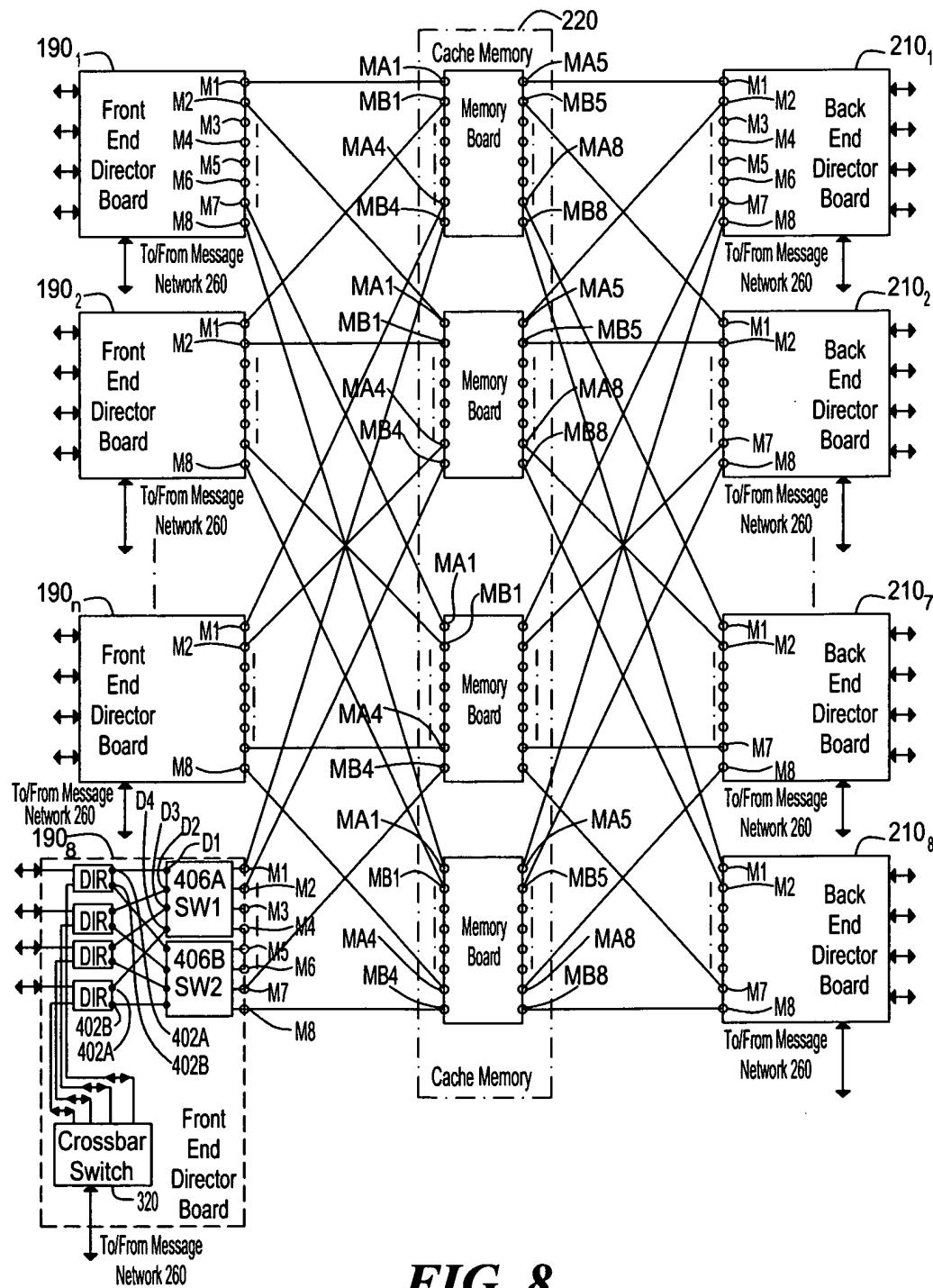
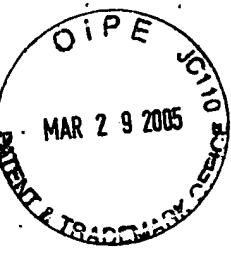
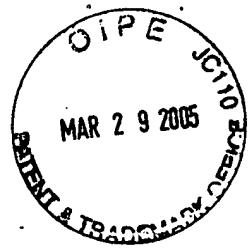


FIG. 8



9/30

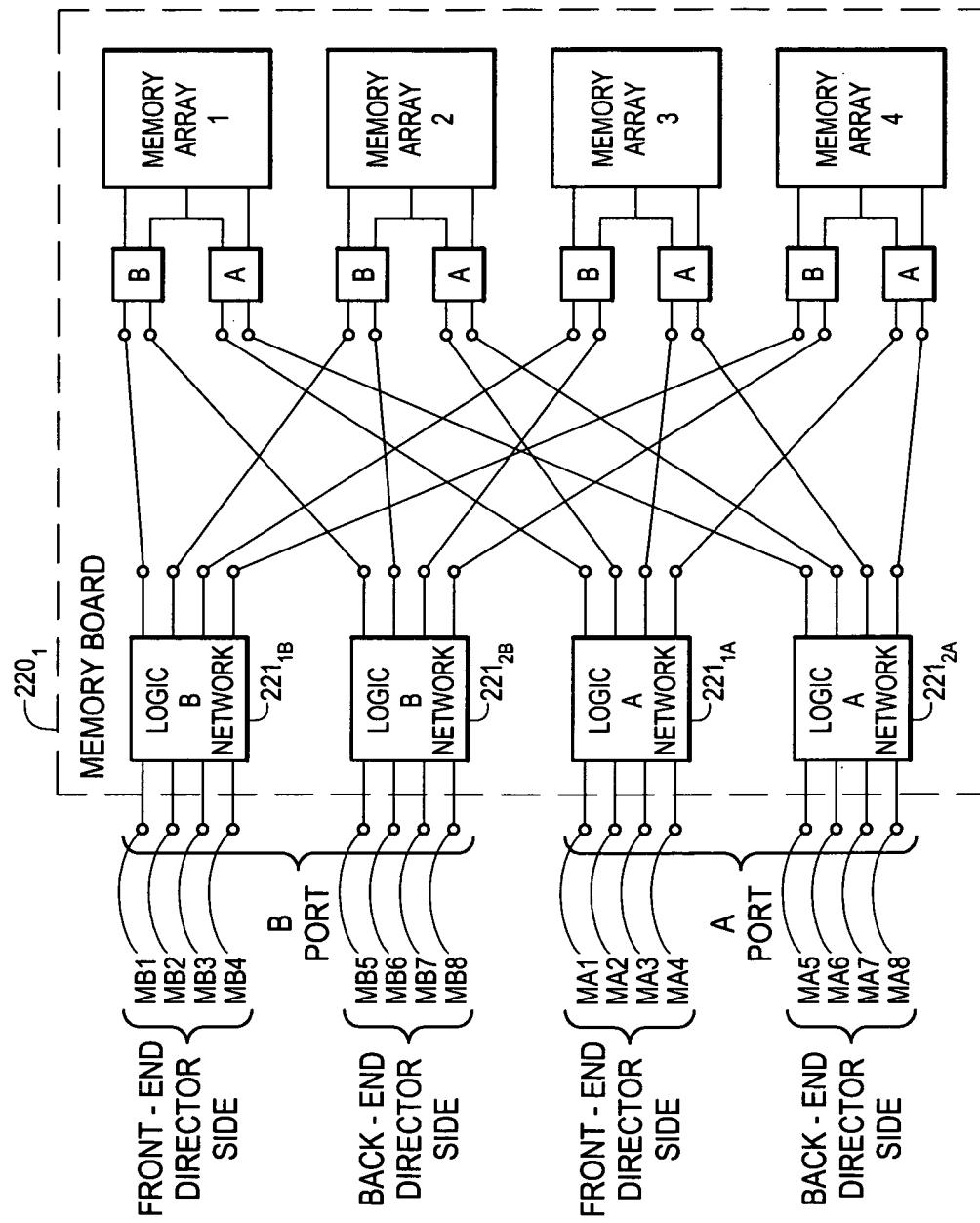
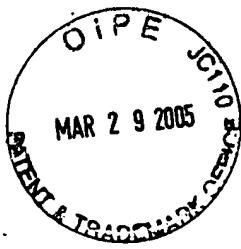


FIG. 8A



10/30

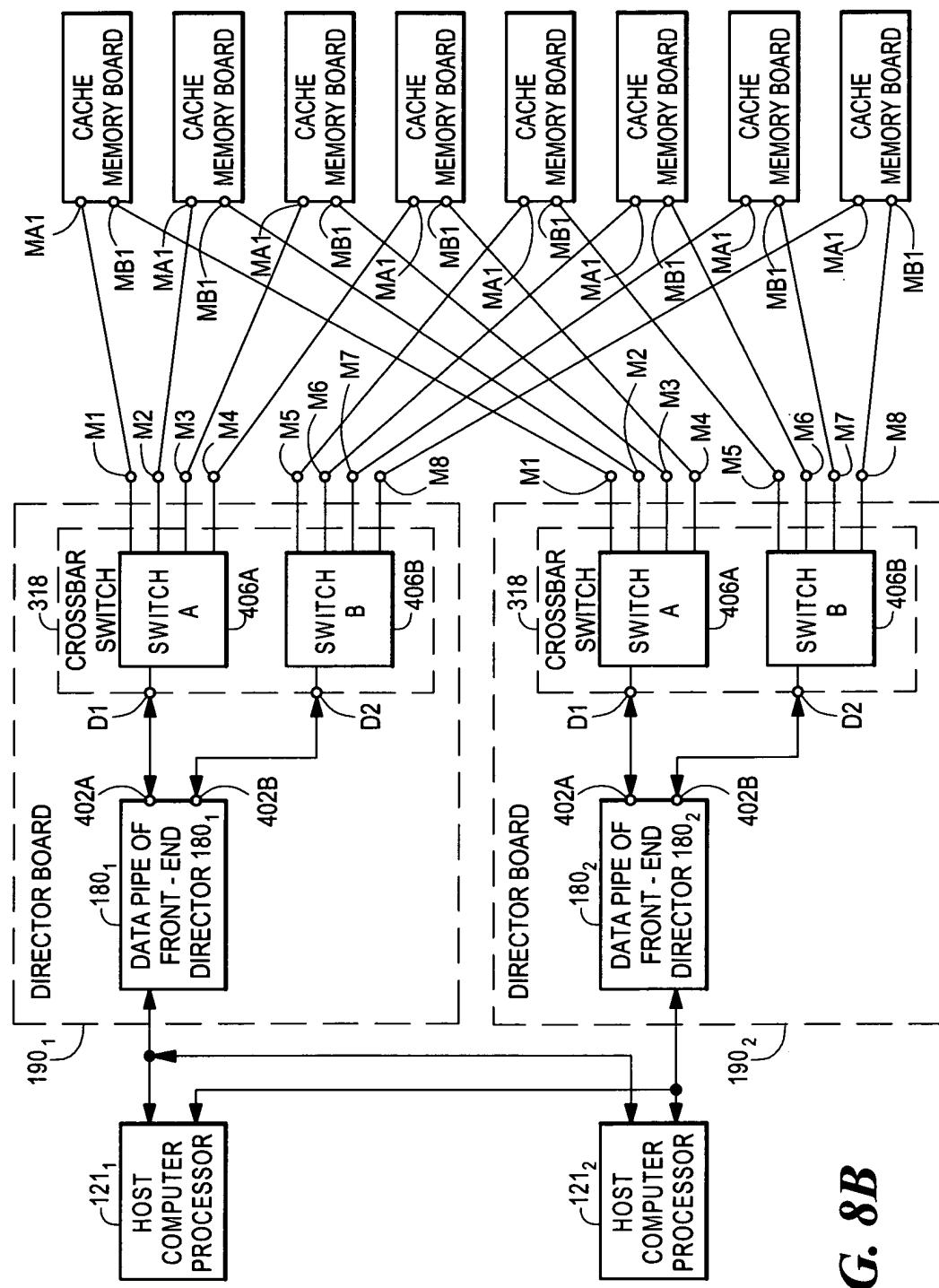


FIG. 8B

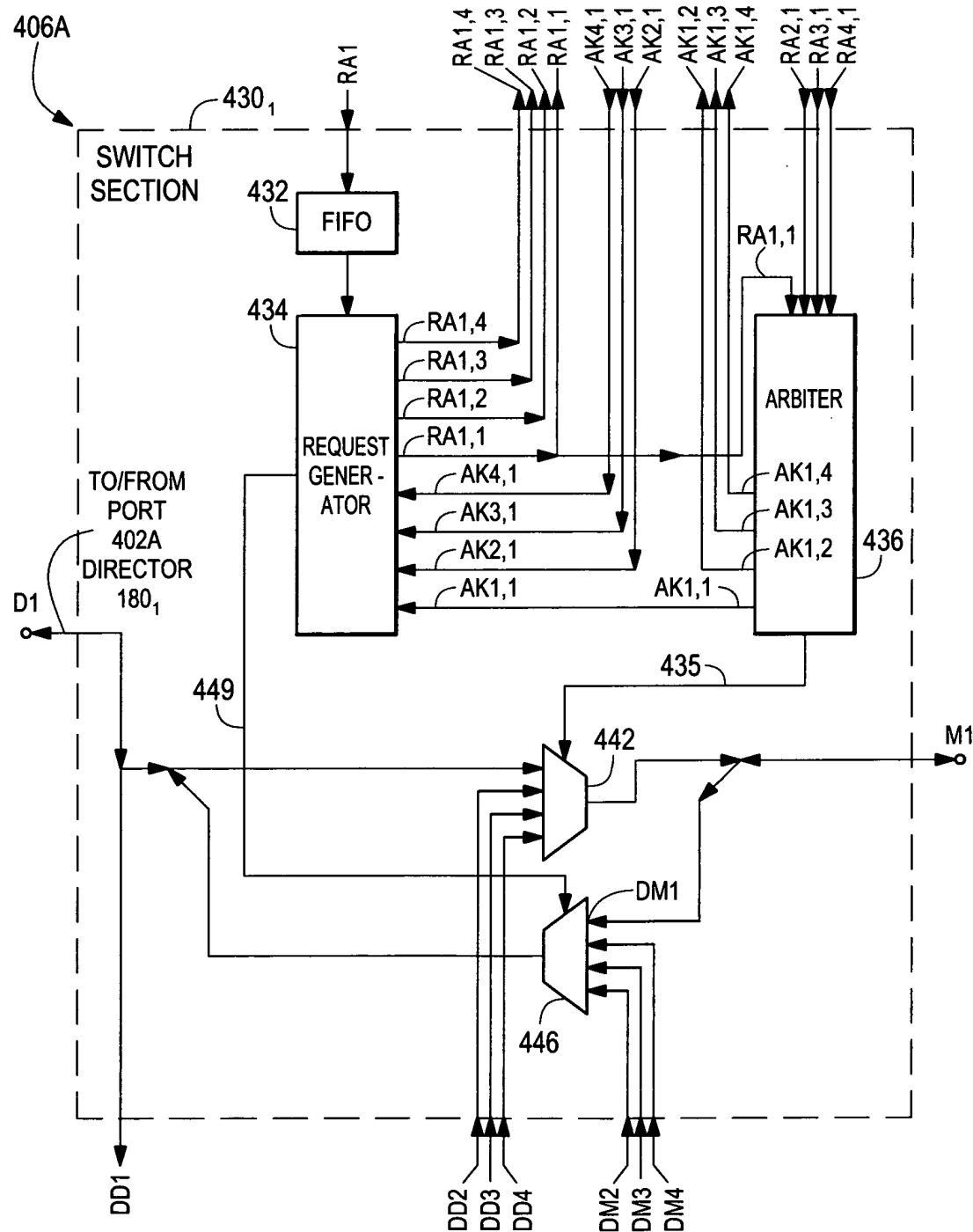
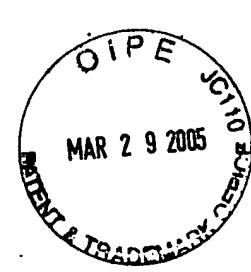


FIG. 8C

FIG. 8C-1

FIG. 8C-1



12/30

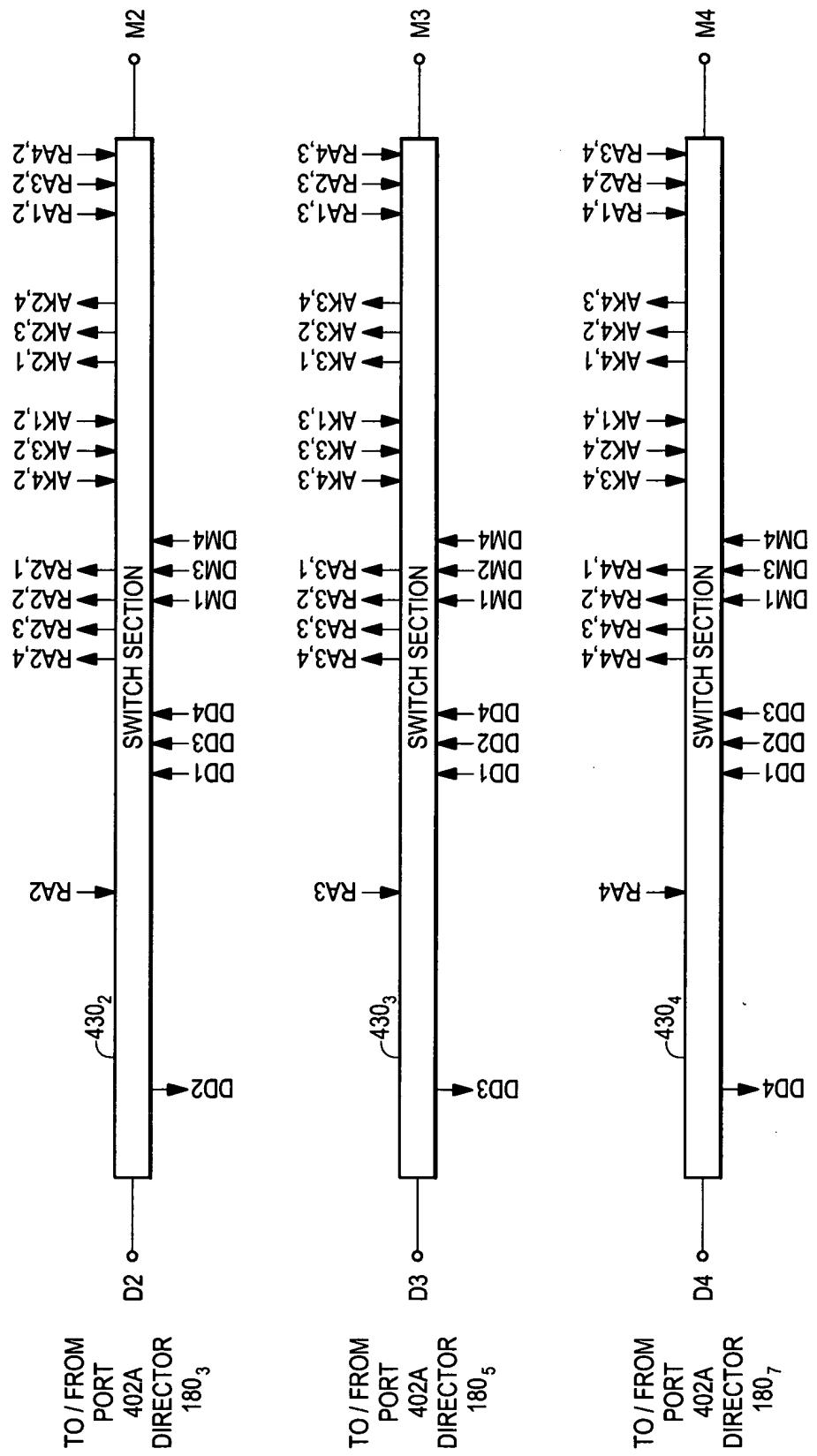
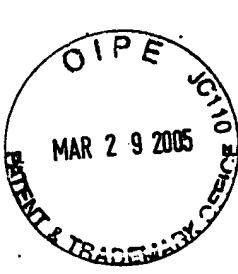


FIG. 8C-2



13/30

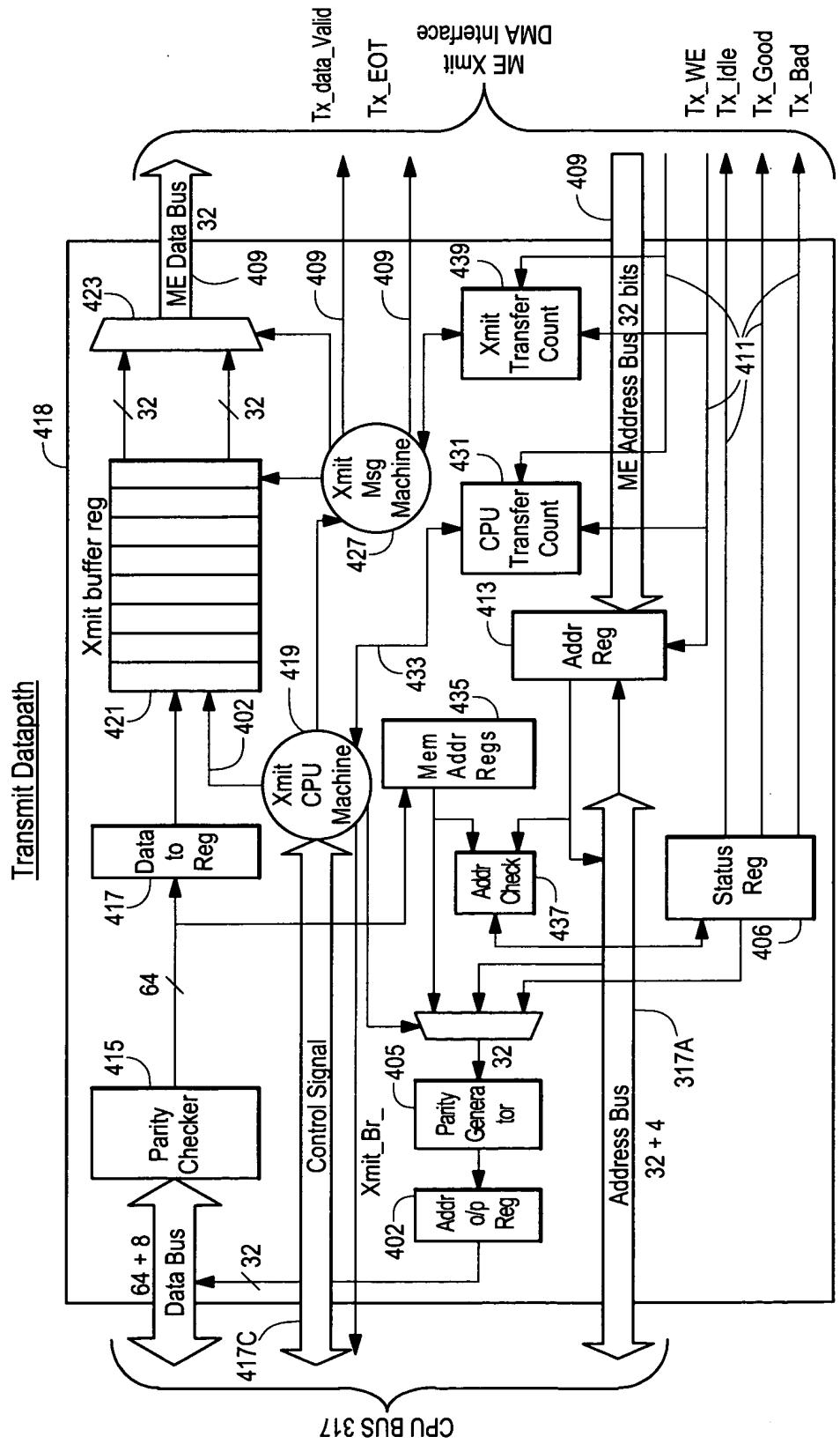


FIG. 9

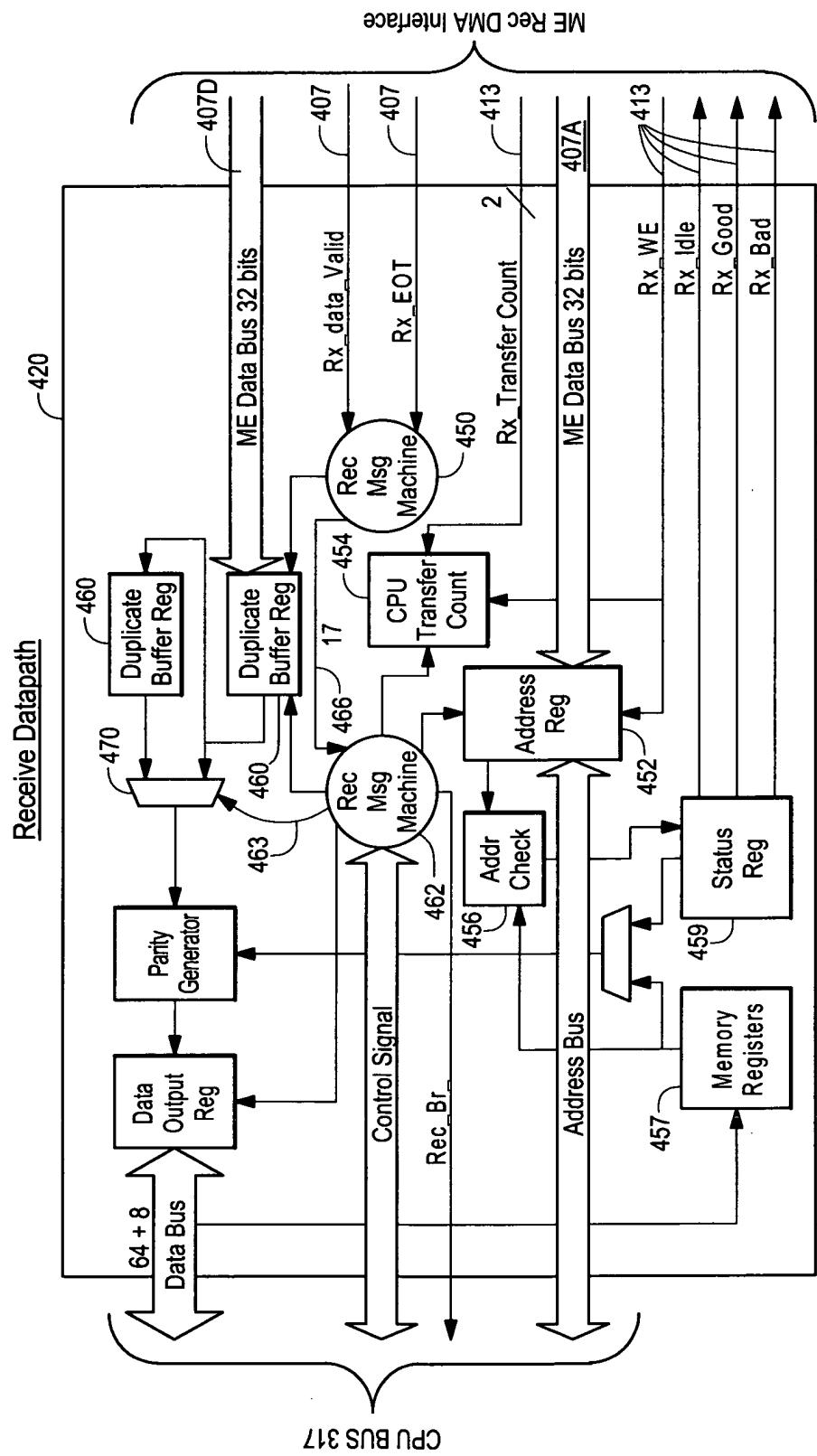
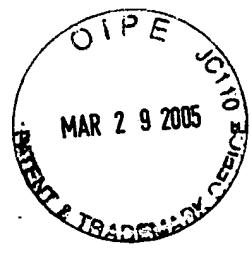


FIG. 10



15/30

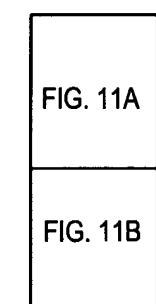


FIG. 11

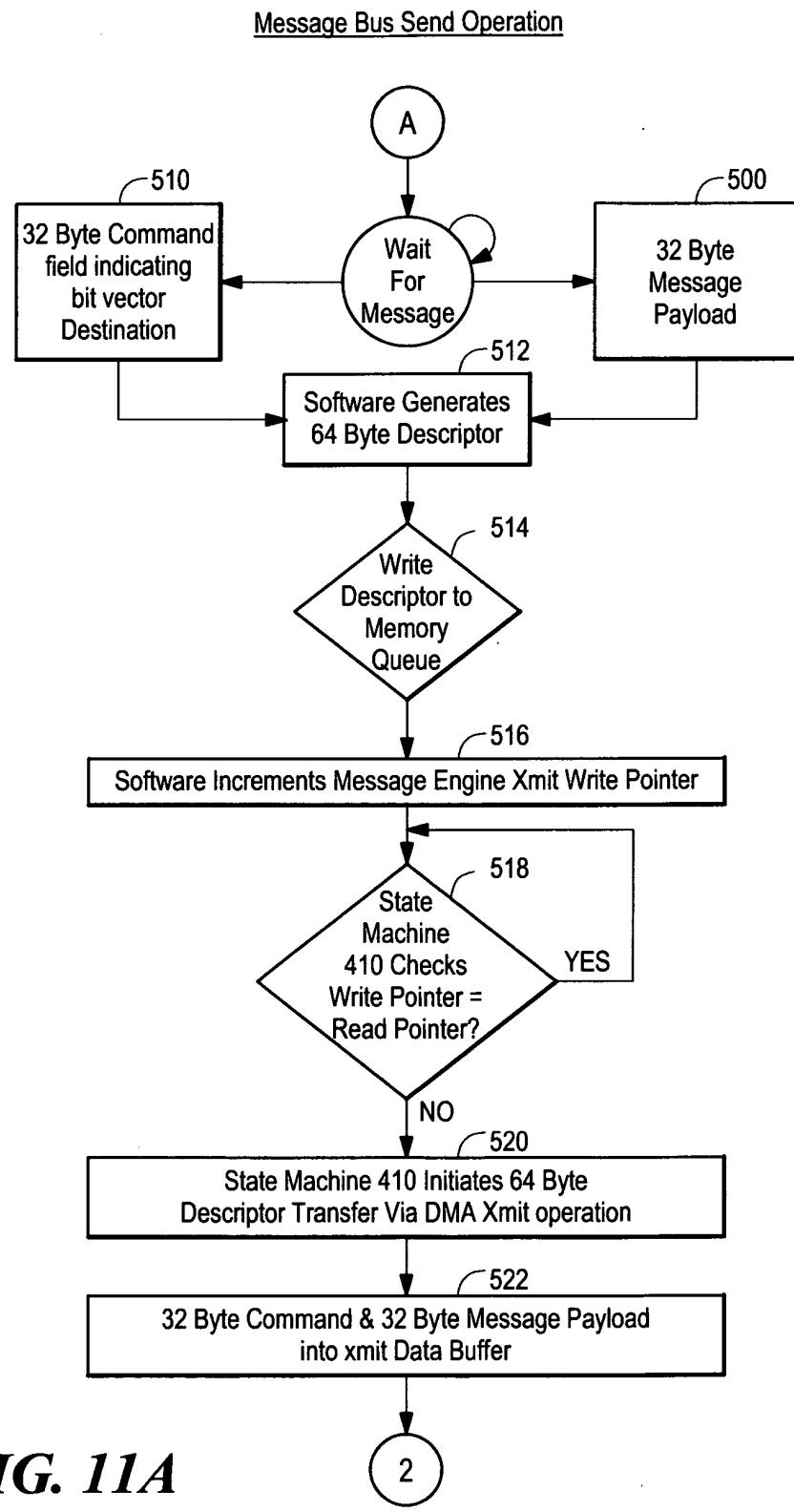


FIG. 11A



16/30

Message Bus Send Operation Continued

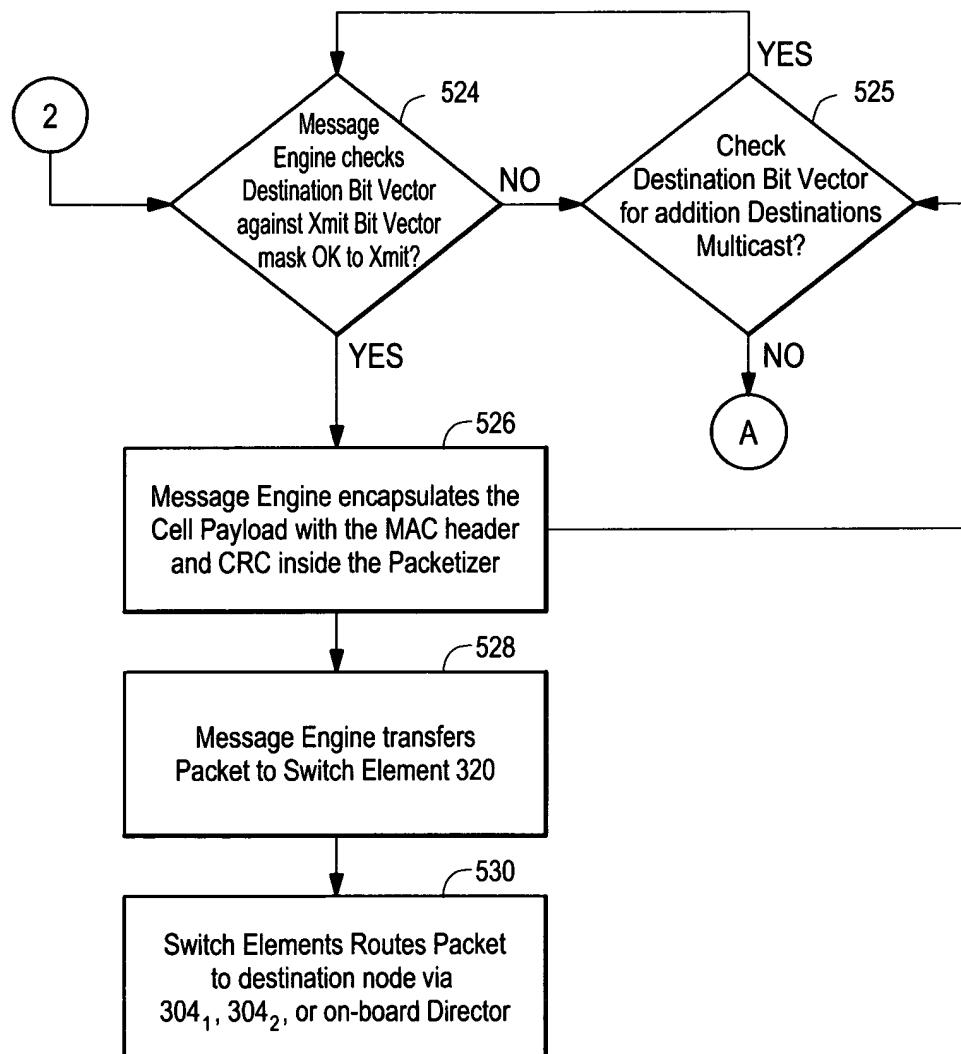
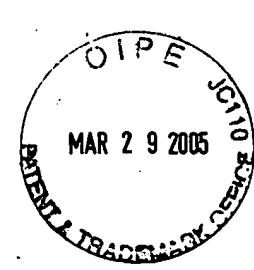


FIG. 11B



17/30

Bit Position	1	2	3	4				62	63	64
	1	0	0	0	-----	-----	-----	0	0	0

FIG. 11C

Bit Position	1	2	3	4				62	63	64
	0	1	0	0	-----	-----	-----	0	0	0

FIG. 11D

Bit Position	1	2	3	4				62	63	64
	0	1	1	0	-----	-----	-----	0	1	1

FIG. 11E

Bit Position	1	2	3	4				62	63	64
	1	1	1	1	-----	-----	-----	1	1	0

FIG. 11F

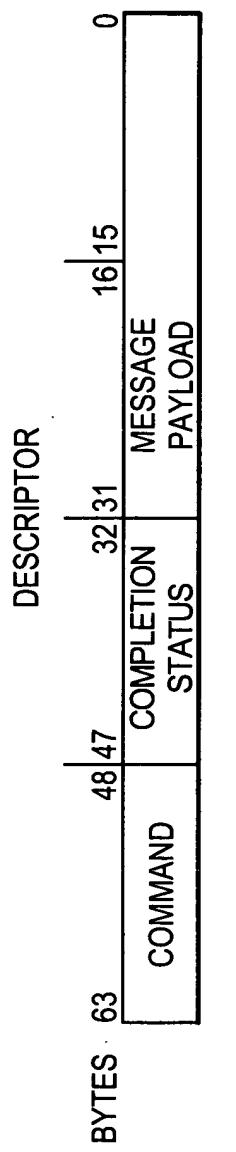
Bit Position	1	2	3	4				62	63	64
	0	1	1	0	-----	-----	-----	0	1	0

FIG. 11G

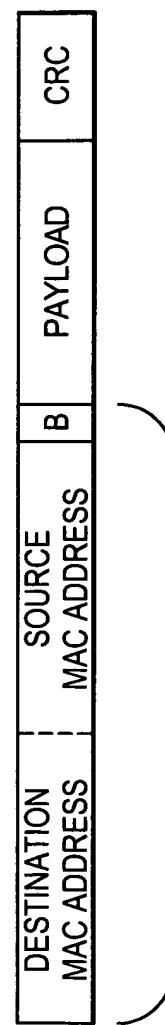


18/30

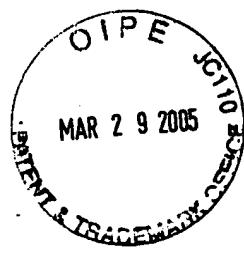
FIG. 2A



MAC PACKET

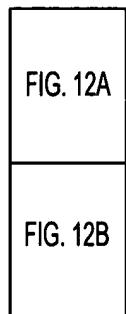


MAC HEADER



19/30

FIG. 12



Message Bus Receive Operation

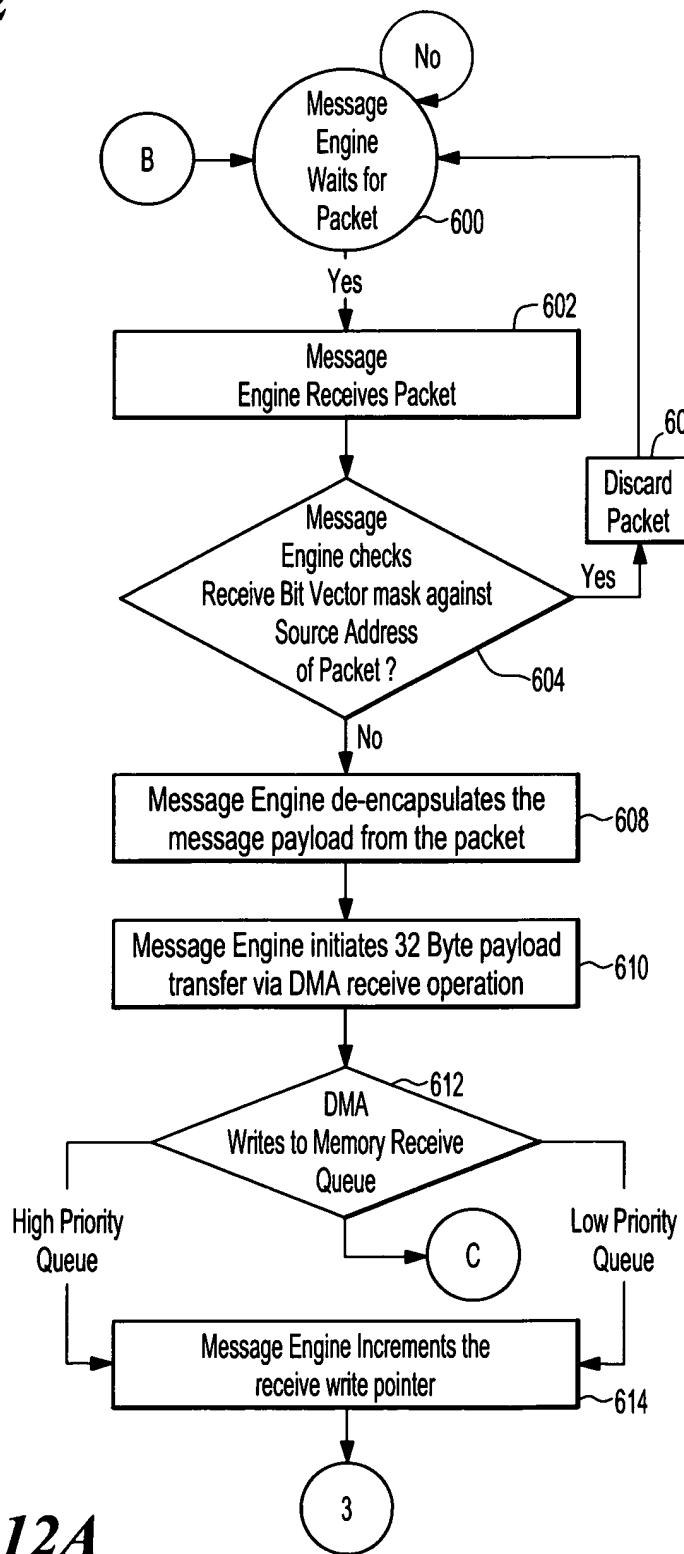
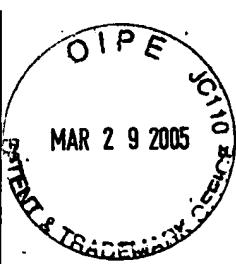


FIG. 12A



20/30

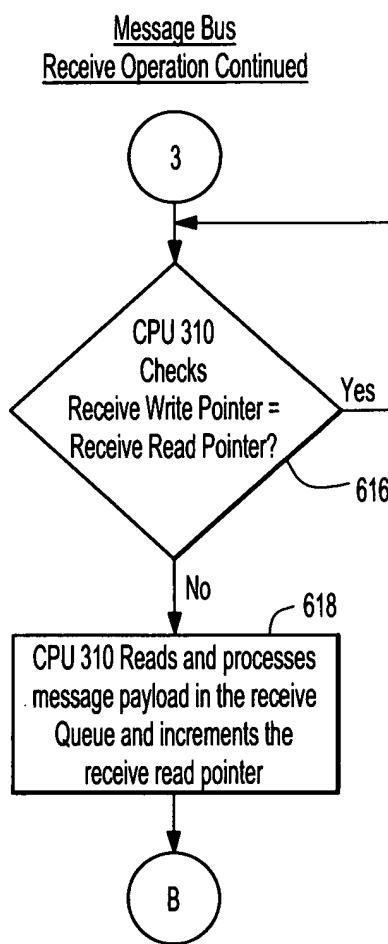


FIG. 12B

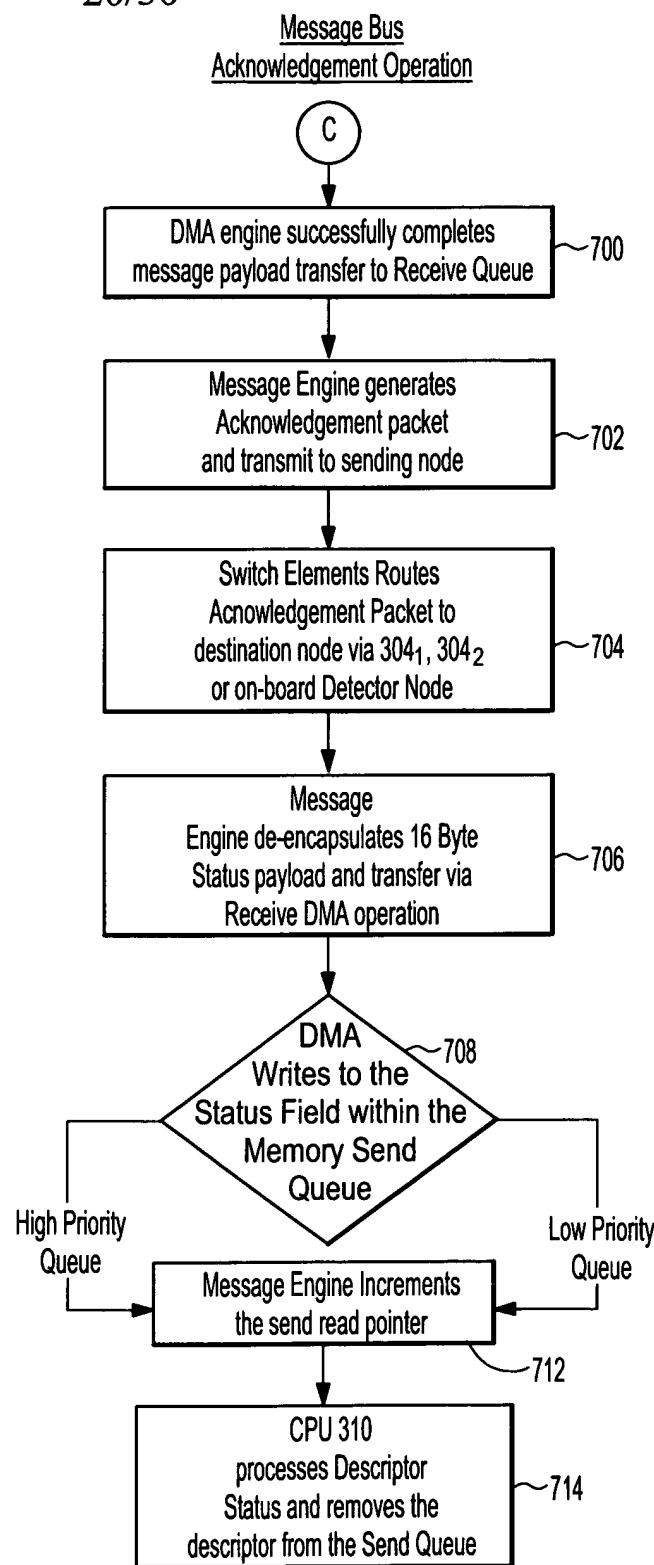


FIG. 13

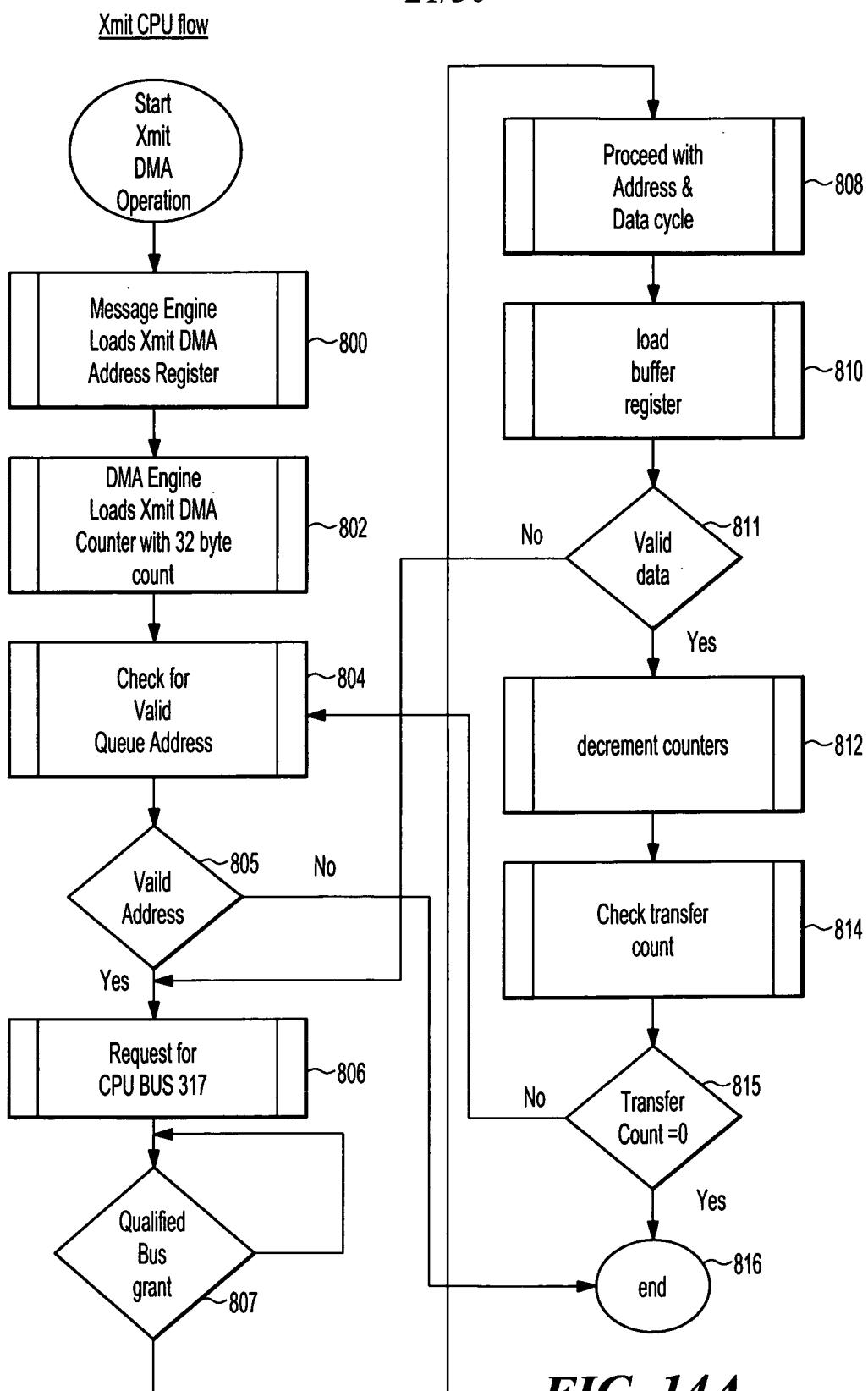
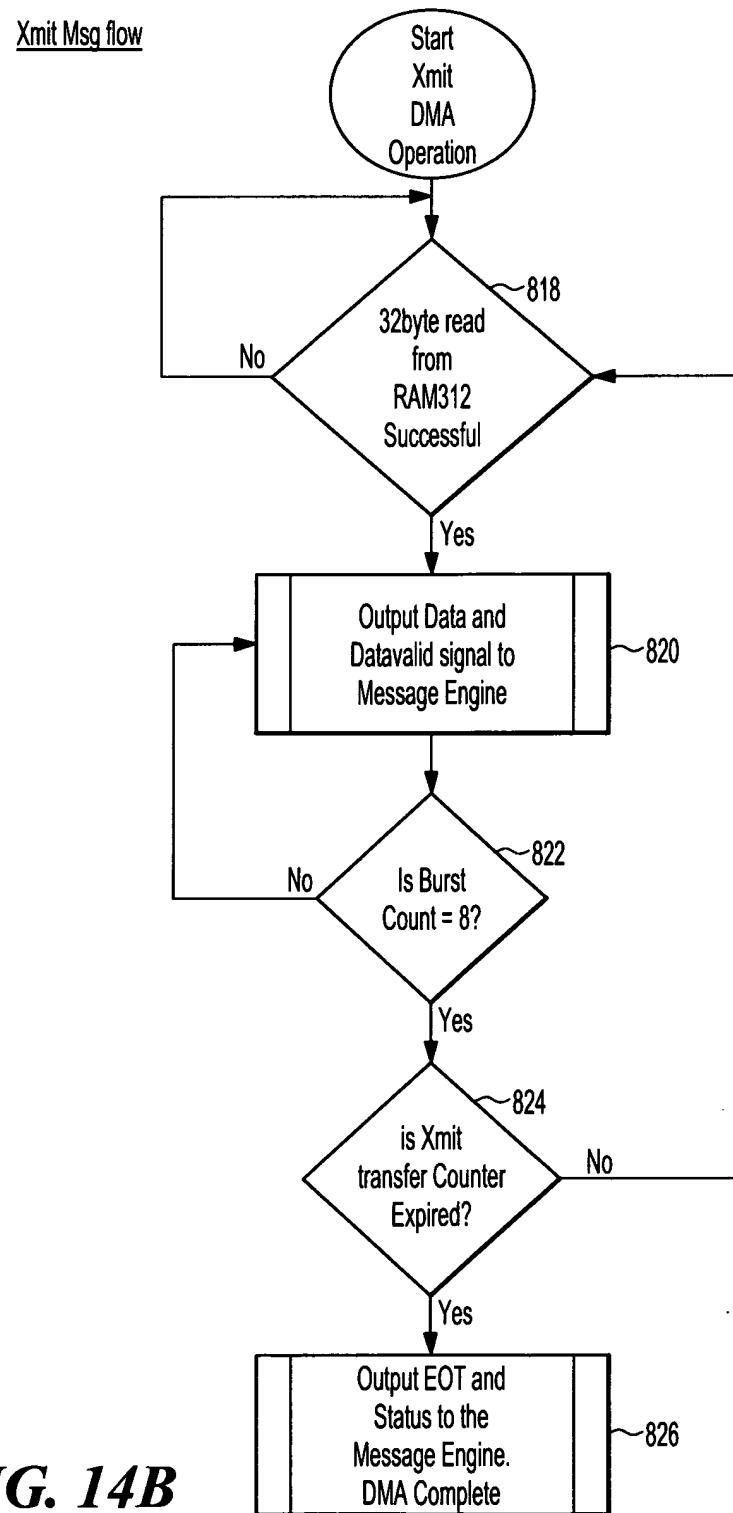


FIG. 14A

**FIG. 14B**

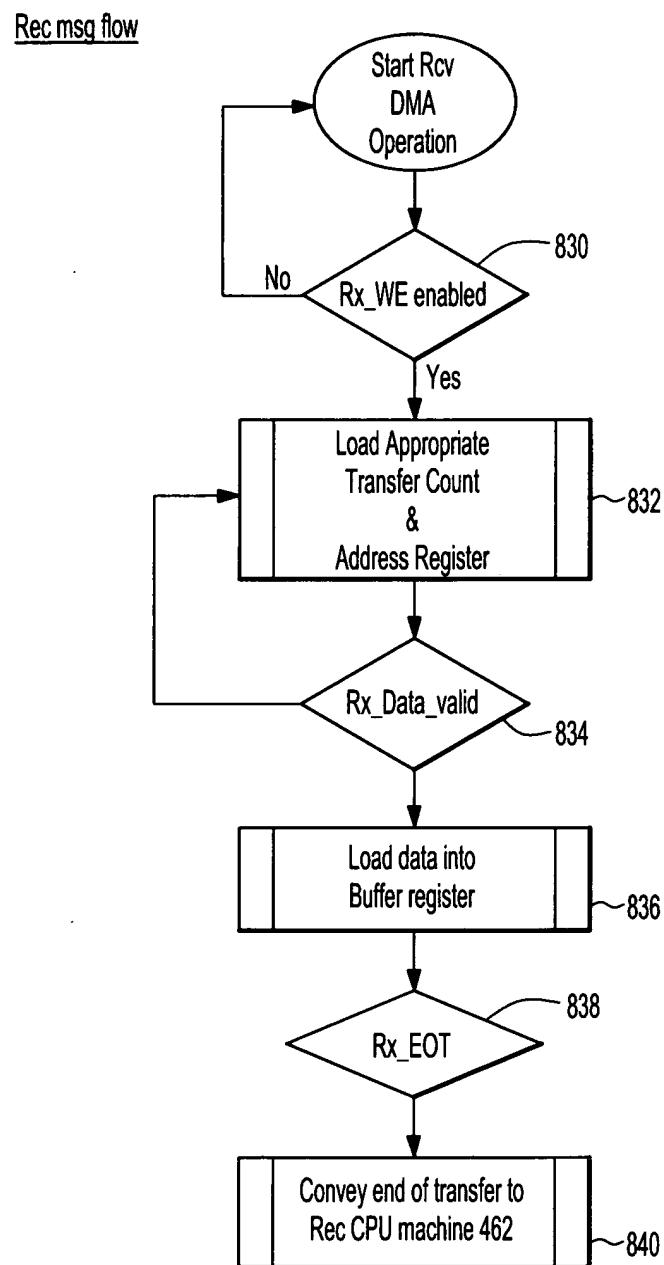
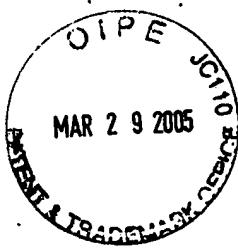


FIG. 15A



24/30

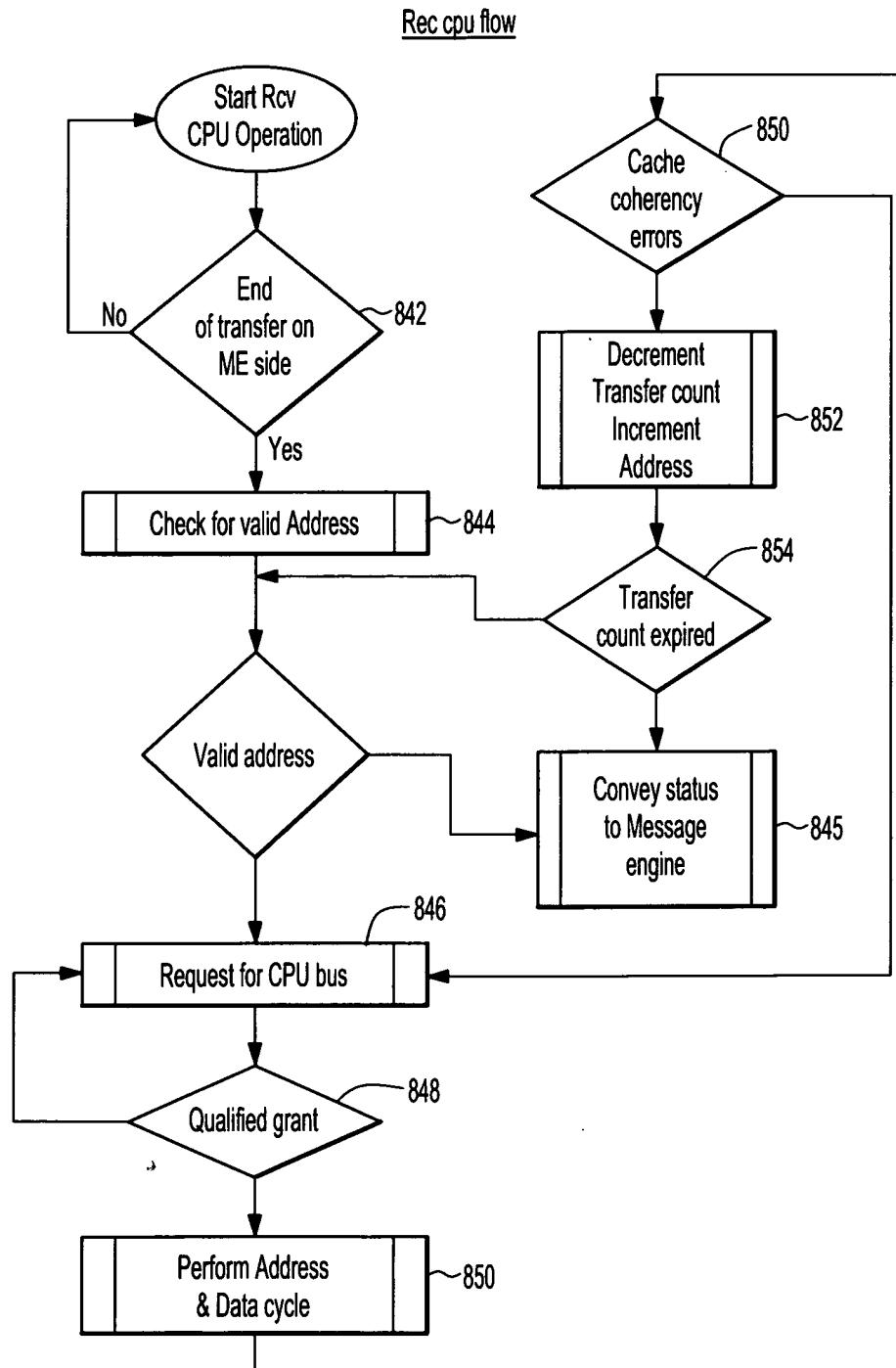


FIG. 15B

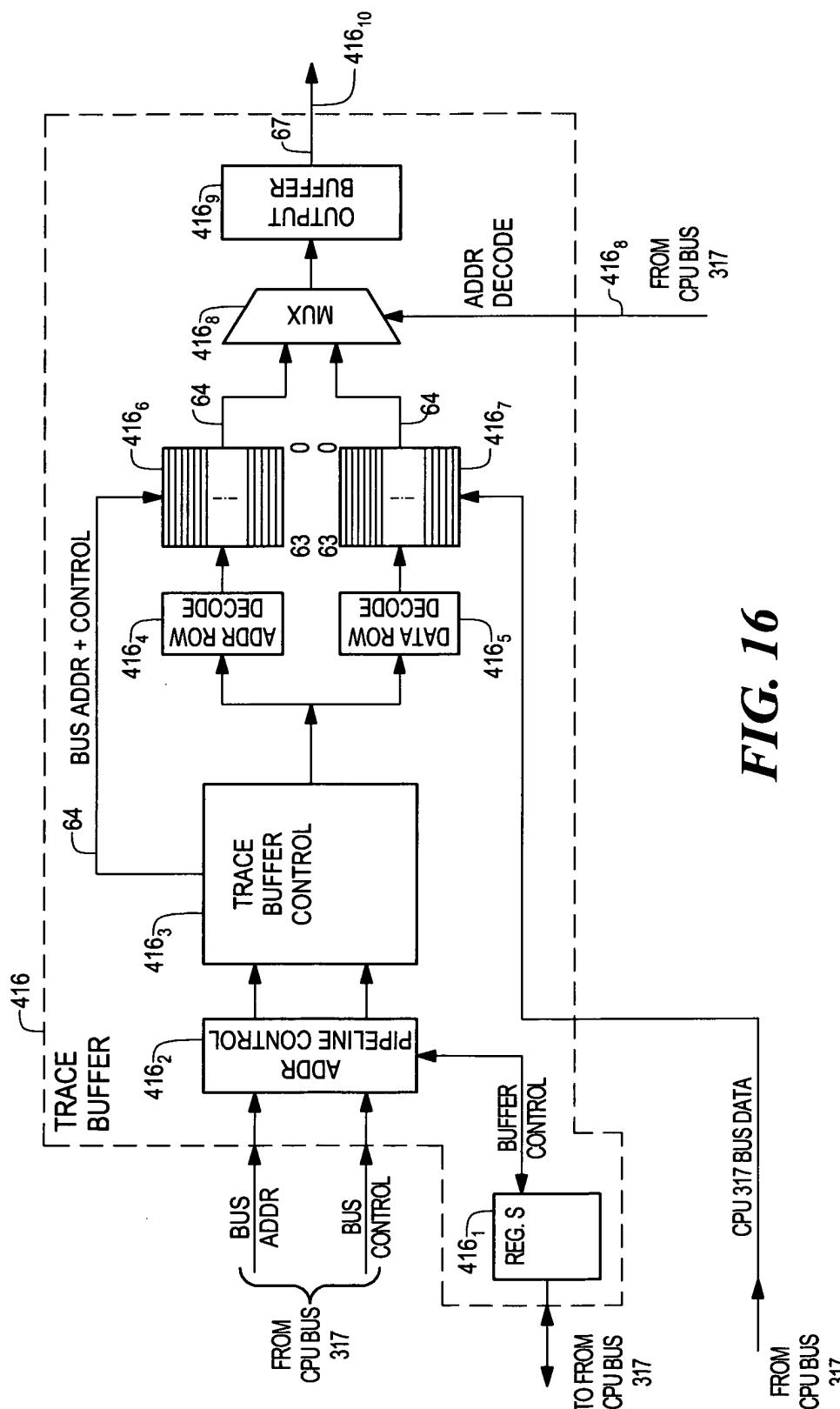


FIG. 16

O I P E
MAR 29 2005

26/30

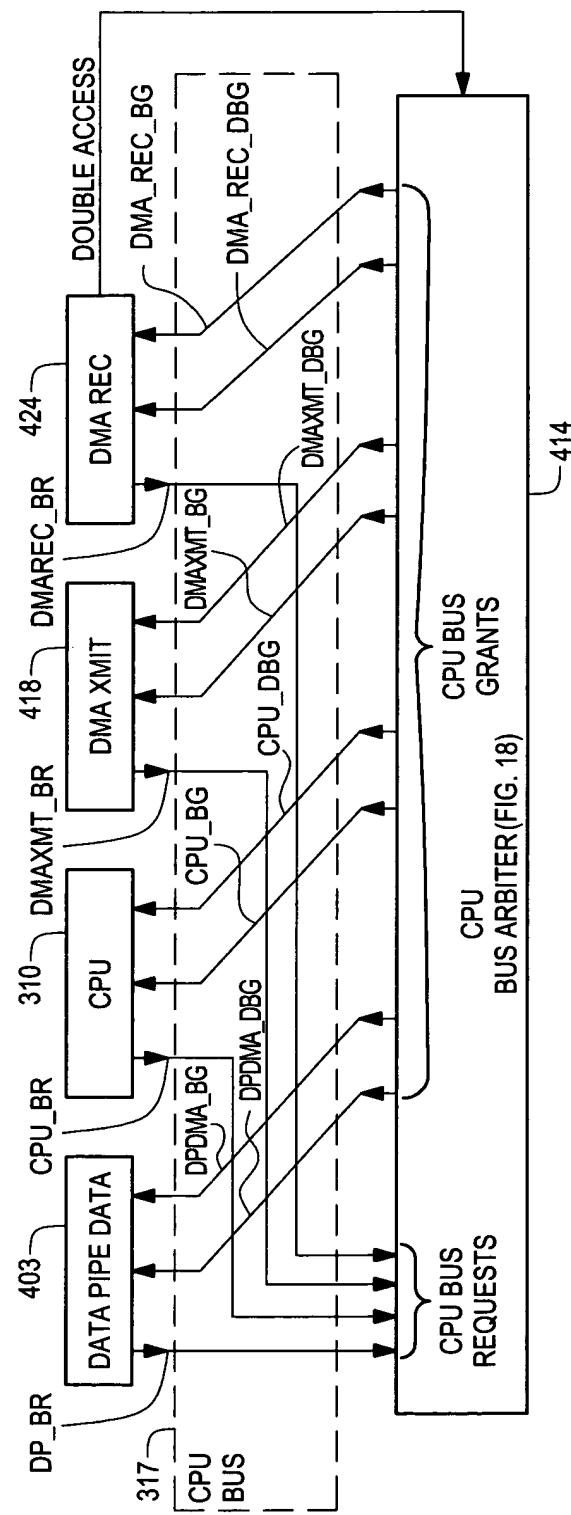
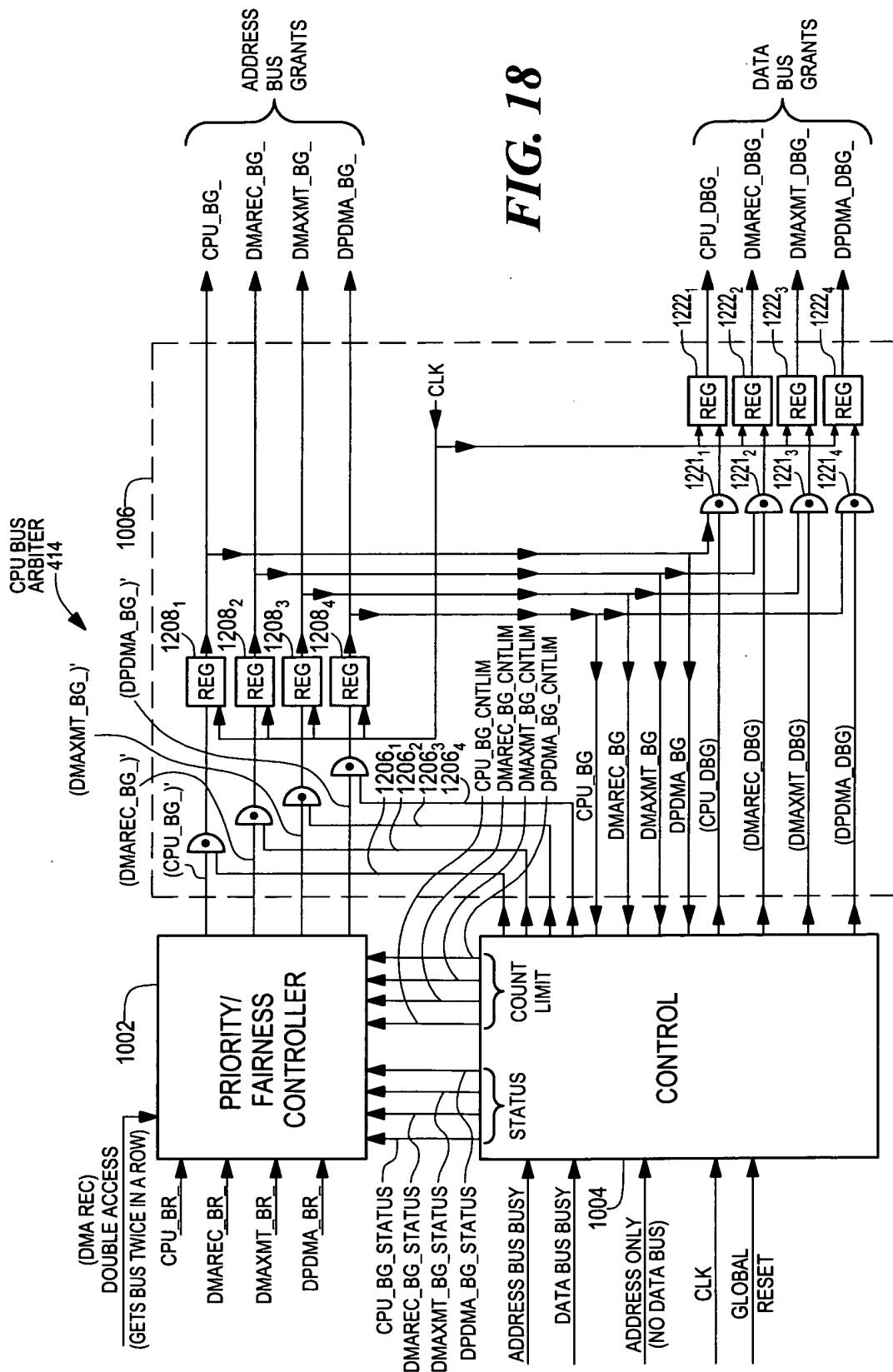


FIG. 17



27/30

FIG. 18

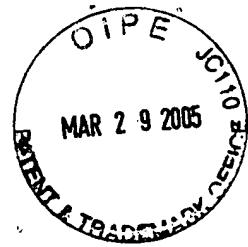


O I P E
MAR 29 2005

28/30

POTENTIAL GRANT TO	CPU- BR	DMAREC- BR	DMAXMT- BR	DPPDMA- BR	CPU_BG- STATUS	DMAREC_BG- STATUS	DMAXMT_BG- STATUS	DPPDMA_BG- STATUS	CPU_BG- CNTLM	DMAREC_BG- CNTLM	DMAXMT_BG- CNTLM	DPPDMA_BG- CNTLM	DOUBLE ACCESS
(CPU_BG)'	DC	0	0	0	DC	DC	DC	DC	DC	DC	DC	DC	DC
(CPU_BG)'	1	DC	DC	0	DC	DC	DC	DC	0	0	0	0	0
(CPU_BG)'	1	DC	DC	DC	DC	DC	DC	DC	1	DC	DC	DC	0
(DMAREC_BG)'	0	1	0	0	DC	DC	DC	DC	DC	DC	DC	DC	DC
(DMAREC_BG)'	DC	1	DC	DC	DC	1	DC	DC	DC	DC	DC	DC	1
(DMAREC_BG)'	0	1	DC	DC	DC	0	DC	DC	DC	0	0	0	DC
(DMAREC_BG)'	1	DC	DC	1	DC	DC	DC	DC	0	DC	0	0	DC
(DMAREC_BG)'	DC	1	DC	DC	DC	DC	DC	DC	0	1	DC	DC	DC
(DMAXMT_BG)'	0	0	1	0	DC	DC	DC	DC	0	DC	0	0	DC
(DMAXMT_BG)'	0	0	1	DC	DC	0	DC	DC	DC	DC	0	0	DC
(DMAXMT_BG)'	0	1	1	DC	DC	1	DC	DC	DC	DC	DC	0	0
(DMAXMT_BG)'	1	0	1	DC	1	DC	DC	DC	DC	DC	DC	0	DC
(DMAXMT_BG)'	DC	DC	1	DC	DC	DC	DC	DC	0	0	1	DC	0
(DPPDMA_BG)'	0	0	0	1	DC	DC	DC	DC	DC	DC	DC	DC	DC
(DPPDMA_BG)'	0	0	1	1	DC	DC	1	0	DC	DC	DC	DC	DC
(DPPDMA_BG)'	0	1	0	1	DC	1	DC	DC	DC	DC	DC	DC	0
(DPPDMA_BG)'	1	0	0	1	1	DC	DC	DC	DC	DC	DC	DC	DC
(DPPDMA_BG)'	DC	DC	1	DC	DC	DC	DC	0	0	0	1	0	0

FIG. 19



29/30

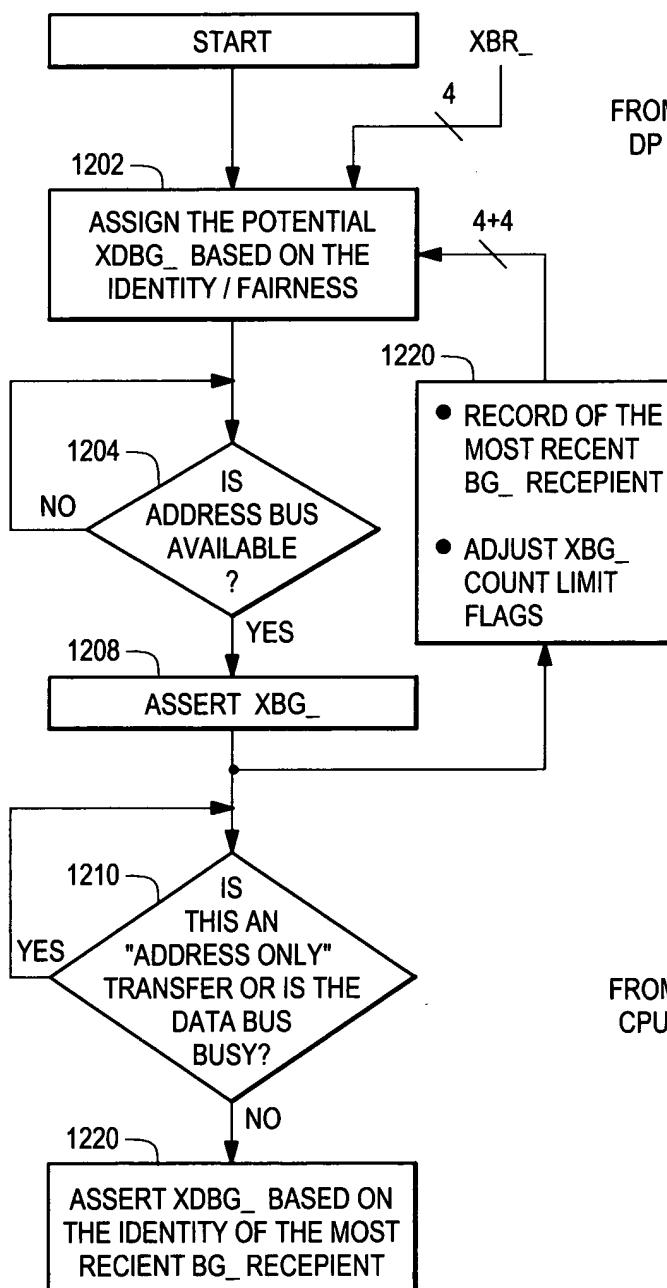


FIG. 20

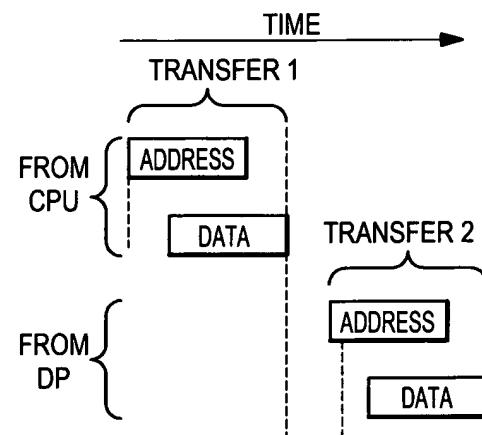


FIG. 21A

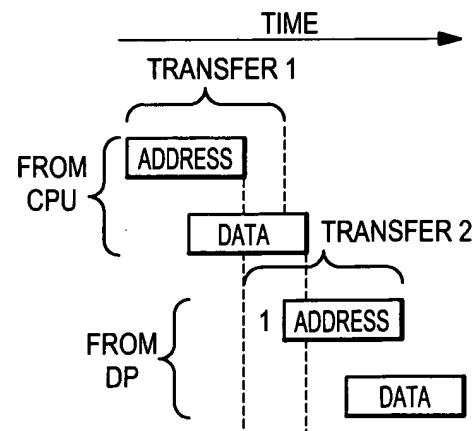


FIG. 21B



30/30

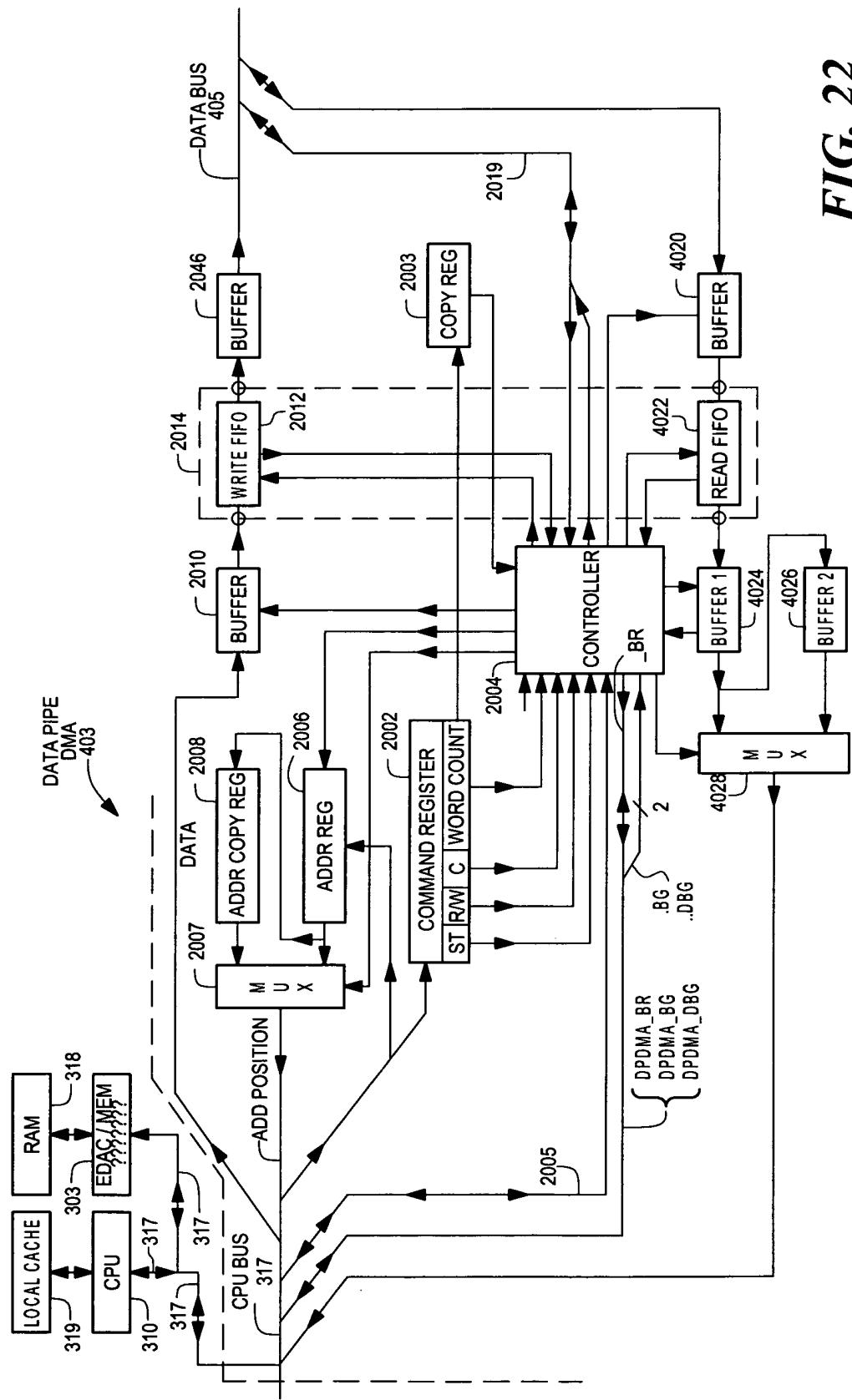


FIG. 22